REMARKS

Applicant is in receipt of the Office Action mailed October 5, 2005. Claims 5, 23, and 85 have been amended. Claims 1-108 remain pending in this case. Reconsideration of the present case is earnestly requested in light of the following remarks.

Priority

In the Office action of October 5, 2005, the Examiner asserts that the disclosure of the prior-filed application, Application No. 09/229,695, fails to provide adequate support under 35 U.S.C. 112, first paragraph, for one or more claims of this application. The Examiner further asserts that the claims as a whole are directed toward a different invention; more specifically, the Examiner was unable to find support for creating a block diagram as recited in claim 1. Applicant respectfully submits that the prior-filed application does provide support for the claims in the instant application.

Applicant notes that the instant application discloses that various portions of a graphical program may be compiled onto various software and hardware elements. For example, 4:30-5:9 recites:

> Alternatively, a user may create a graphical program in a graphical programming environment which allows the user to select, manipulate, and interconnect graphical icons. The graphical icons represent a variety of processing operations, functions, and/or transformations which may be of interest to the user such as signal processing blocks, standard software operations, hardware devices, circuits, elements, etc. The user thus builds a graphical program which represents a desired test system architecture. Various portions of the graphical program may then be compiled into one or more of (1) software for execution on the host processor, (2) software for execution on the embedded processor in the RTI, (3) configuration information to be downloaded to the reconfigurable hardware of the RTI, i.e. the reconfigurable hardware module, and/or the reconfigurable front end.

Applicant also notes that the incorporated reference, U.S. Patent No. 6,219,628, discloses block diagrams in relation to graphical programs in numerous locations. For example, in 11:56-57, 6,219,628 discloses "the user creates a graphical program, sometimes referred to as a block diagram".

Applicant notes further that the Examiner states, in the section 103 rejections of the current Office Action, "Fountain teaches National Instruments LabVIEW, which teaches the use of block diagrams for a familiar technique and to enable rapid building, testing and modyfing...". Applicant respectfully submits that the instant application refers to LabVIEW throughout the specification as one example of the hardware design utility.

Thus, Applicant submits that creating a block diagram is supported by the specification in the instant application.

Objections

The Examiner objected to claim 5 because of an informality. Specifically, claim 5, line 9 ended with a period. Claim 5 has been amended to address this issue.

The Examiner also objected to claims 1-108. As an example, the Examiner noted that claim 1 recites both "programmable hardware element" and "reconfigurable circuitry". The Examiner requested clarification on what separates the metes and bounds between these two elements.

Applicant notes that the paragraph beginning on page 3, line 13 recites:

> The problems outlined above are largely resolved by the reconfigurable test system and method of the present invention. The reconfigurable test system includes a host computer coupled to a reconfigurable test instrument (RTI). The RTI is configured for coupling to a unit under test through a communication medium. The RTI preferably includes a reconfigurable hardware module, a reconfigurable front end, and optionally an embedded processor with local memory. The reconfigurable hardware module preferably includes one or more reconfigurable or programmable hardware devices such as Field Programmable Gate Arrays (FPGAs). Thus, the reconfigurable hardware module may be programmed to realize any desired hardware architecture. The reconfigurable front end preferably includes programmable transceivers which may be programmed to interface with any desired types of signals using any desired line encoding scheme, voltage levels, etc.

Applicant respectfully submits that cited paragraph defines the metes and bounds of programmable hardware element and reconfigurable circuitry. For example, as the cited paragraph indicates, and as is well known in the art, a programmable hardware element, e.g., an FPGA, may be configured to implement virtually any functionality

desired, e.g., any desired hardware architecture, whereas reconfigurable circuitry, e.g., a programmable transceiver, implements a specific functionality, but may be configured or programmed to perform that functionality in a variety of ways.

Thus, Applicant respectfully submits that the objection is improper, and requests removal of the objection to claims 1-108.

Information Disclosure Statement

Applicant notes that the Examiner was unable to locate the non-patent references listed in the IDS of June 27, 2002, and that these references cannot be found in the parent case. These references were provided for the parent case, but have apparently been lost. Applicant has thus resubmitted the non-patent references herewith, and requests that the Examiner consider them fully.

Section 112 Rejections

Claim 23 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 23 has been amended to depend from claim 22. Removal of the 112 rejection is therefore requested.

Section 103 Rejections

Claims 1-108 were rejected under 35 U.S.C. 103(a) as being unpatentable over A Software Development System for FPGA-Based Data Acquisition Systems by Wenban et al. ("Wenban") in view of Software Advances in Measurement and Instrumentation, by Fountain ("Fountain").

Regarding claim 1, Applicant respectfully submits that Wenban in view of Fountain fails to teach or suggest **wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element**. The Examiner has cited the Abstract and Conclusion of Wenban. The Abstract of Wenban recites:

> We present a compiler, debugger, linker, and hardware/software interface for data acquisition systems based on hardware that is reconfigurable by the end user. Unlike earlier work, we choose a source language which is software-oriented. Our goal is to make systems with reconfigurable

hardware accessible to scientists and engineers who are competent programmers but are not hardware literate.

Similarly, the Conclusion of Wenban recites: "We have presented a suite of tools, including a compiler, a debugger, a linker, and interfaces, which support a software-oriented view of reconfigurable hardware". Wenban goes on to describe two trial applications which utilize FPGAs: a data acquisition card and a reconfigurable network node. Applicant respectfully submits that Wenban nowhere teaches reconfigurable circuitry coupled to the programmable hardware element. For example, Wenban's reconfigurable network node "is a standalone board with an FPGA, a bootstrap loader PLD, SRAM, ROM, and network line drivers and receivers" (page 36, left column, second paragraph). Similarly, Wenban's data acquisition card "is an ISA compatible board featuring a large FPGA, two banks of high-speed static RAM, and two external I/O connectors" (page 35, left column, second paragraph). Applicant notes that Wenban nowhere mentions reconfigurable circuitry coupled to the programmable hardware element in his description of either the data acquisition board or the reconfigurable network node. Thus, Wenban fails to teach or suggest this feature. Nor does Fountain disclose this feature of claim 1.

In further regard to claim 1, Wenban in view of Fountain fails to teach or suggest **configuring the reconfigurable circuitry in the device**. In asserting that the cited references teach this feature, the Examiner cites Wenban, page 36, left column, second paragraph, specifically "A complete FPGA configuration file can be downloaded over the network into the SRAM using these messages". Applicant respectfully submits that the FPGA in Wenban is not reconfigurable circuitry coupled to a programmable hardware element, as recited in claim 1 of the instant application. As argued above, Wenban fails to disclose reconfigurable circuitry coupled to the programmable hardware element. Therefore, Applicant respectfully submits that Wenban fails to teach or suggest *configuring the reconfigurable circuitry in the device.*

The Examiner admits that "Wenban does not expressly teach that the computer program is written as a block diagram", but asserts that "it would have been obvious to

one of ordinary skill in the art at the time of Applicant's invention to combine the graphical programming of Fountain with the development environment of Wenban", suggesting the motivation: "to create a familiar technique and to enable rapid building, testing and modifying on Fountain on page 8".

Applicant reminds the Examiner, as held by the U.S. Court of Appeals for the Federal Circuit in Ecolochem Inc. v. Southern California Edison Co., an obviousness claim that lacks evidence of a suggestion or motivation for one of skill in the art to combine prior art references to produce the claimed invention is defective as hindsight analysis.

In addition, the showing of a suggestion, teaching, or motivation to combine prior teachings "must be clear and particular . . .. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'." *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). The art must fairly teach or suggest to one to make the specific combination as claimed. That one achieves an improved result by making such a combination is no more than hindsight without an initial suggestion to make the combination.

Applicant respectfully submits that the Examiner's suggested motivation to combine: "to create a familiar technique and to enable rapid building, testing and modifying", simply describes utility of the National Instruments LabVIEW environment, i.e., is simply a statement of perceived benefits of graphical programming in general, and nowhere suggests the alleged combination. More specifically, Applicant submits that neither reference teaches or suggests to one to make ***the specific combination as claimed.*** Thus, for at least the reasons provided above, Applicant submits that the Examiner's motivation is improper.

Applicant also respectfully submits that, as argued above, Wenban and Fountain, taken singly or in combination, fail to teach or suggest *wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element* and *configuring the reconfigurable circuitry in the device.* In fact, Fountain nowhere mentions or even hints at reconfigurable circuitry or programmable hardware elements. Nor does Wenban

mention using graphical programs. Nor does either reference disclose reconfigurable circuitry coupled to a programmable hardware element at all.

Thus, even if Wenban and Fountain were properly combinable, which Applicant argues they are not, the combination would not teach or suggest all the features and limitations of claim 1.

Thus, for at least the reasons provided above, Applicant submits that Wenban and Fountain, taken singly or in combination, fail to teach all the features and limitations of claim 1, and so Applicant submits that claim 1, and those claims dependent therefrom, are patentably distinct and non-obvious over the cited art, and are thus allowable.

Claims 24, 25, 27, 31, 64, and 86 include similar limitations as claim 1, and so the above arguments apply with equal force to these claims. Thus, for at least the reasons provided above, Applicant submits that claims 24, 25, 27, 64, and 86, and those claims respectively dependent therefrom, are patentably distinct and non-obvious, and are thus allowable.

Regarding claim 4, Applicant submits that Wenban in view of Fountain nowhere teaches or suggests *wherein said generating comprises generating the hardware architecture file based on the first portion of the block diagram and wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry based on the second portion of the block diagram.* As argued above, Wenban nowhere discloses reconfigurable circuitry coupled to a programmable hardware element. Applicant also submits that Wenban nowhere discloses first and second portions of a block diagram (graphical program) to be implemented respectively in the programmable hardware element and the reconfigurable circuitry. The Examiner asserts that pages 8 and 9 of Fountain teach "a modular, multilevel design of various portions, for various hardware items". Applicant respectfully submits that "a modular, multilevel design of various portions, for various hardware items" is not *wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry.*

Thus, for at least the reasons provided above, Applicant submits that claim 4 is patentably distinct and non-obvious, and is thus allowable.

Claim 56 includes similar limitations as claim 4, and so the above arguments apply with equal force to this claim. Thus, for at least the reasons provided above, Applicant submits that claim 56, and those claims respectively dependent therefrom, are patentably distinct and non-obvious, and are thus allowable.

Claim 60 includes similar limitations as claim 4, and so the above arguments apply with equal force to this claim. Applicant submits that Wenban in view of Fountain also fails to teach or suggest the further limitation provided by claim 60: *storing a software program based on the third portion of the block diagram in the memory for execution by the processor.* Applicant respectfully submits that the Examiner has not provided arguments regarding this limitation.

Claim 62 includes similar limitations as claim 60, and so the above arguments regarding claims 1, 4, and 60 apply with equal force to this claim. Applicant submits that Wenban in view of Fountain also fails to teach or suggest the further limitation provided by claim 62: *storing a host software program based on the fourth portion of the block diagram in the host memory for execution by the host processor.* Applicant respectfully submits that the Examiner has not provided arguments regarding this limitation.

Claim 63 includes similar limitations as claim 4, and so the above arguments regarding claims 1 and 4 apply with equal force to this claim. Applicant submits that Wenban in view of Fountain also fails to teach or suggest the further limitation provided by claim 63: *executing a utility to automatically specify a first portion of the block diagram to be implemented in the programmable hardware element and a second portion of the block diagram to be implemented by the reconfigurable circuitry.* Applicant respectfully submits that the Examiner has not provided arguments regarding this limitation. Thus, for at least the reasons provided above, Applicant submits that claims 60, 62, and 63, and those claims respectively dependent therefrom, are patentably distinct and non-obvious, and are thus allowable.

Regarding claim 6, Applicant submits that Wenban in view of Fountain nowhere teaches or suggests *creating a reconfigurable circuitry configuration file based on the*

second block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry. As argued above, Wenban nowhere discloses reconfigurable circuitry coupled to a programmable hardware element. Applicant also submits that Wenban nowhere discloses a reconfigurable circuitry configuration file. As in claim 4, the Examiner cites pages 8 and 9 of Fountain. Similar to the arguments presented above, "a modular, multilevel design of various portions, for various hardware items" is not *creating a reconfigurable circuitry configuration file based on the second block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry.*

Thus, for at least the reasons provided above, Applicant submits that claim 6 is patentably distinct and non-obvious, and is thus allowable.

Claims 26 and 58 include similar limitations as claim 6, and so the above arguments apply with equal force to these claims. Thus, for at least the reasons provided above, Applicant submits that claims 26 and 58, and those claims respectively dependent therefrom, are patentably distinct and non-obvious, and are thus allowable.

Claim 61 includes similar limitations as claim 6, and so the above arguments regarding claims 1 and 6 apply with equal force to this claim. Applicant submits that Wenban in view of Fountain also fails to teach or suggest the further limitation provided by claim 61: *the third block diagram to be implemented by the processor and memory.* Applicant respectfully submits that the Examiner has not provided arguments regarding this limitation. Thus, for at least the reasons provided above, Applicant submits that claim 61, and those claims respectively dependent therefrom, are patentably distinct and non-obvious, and are thus allowable.

Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the rejection has been shown to be unsupported for the independent claims, a further discussion of the dependent claims is not necessary at this time.

Applicant respectfully requests removal of the section 103 rejection of claims 1-108.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-22503/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☒ Copy of 13 non-patent references listed in the IDS of June 27, 2002

Respectfully submitted,

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